Listing of Claims

This listing of claims replaces all prior versions, and listings, of claims.

1. (Currently Amended) A semiconductor integrated circuit apparatus, comprising:

a plurality of electrically conductive vias for electrically connecting metal layers of said apparatus;

a first dielectric layer overlying said vias; ~~and~~

a stress relief layer that is more flexible than said first dielectric layer, said stress relief layer overlying said vias and interposed between said vias and said first dielectric layer; and

a further dielectric layer that is less flexible than said stress relief layer, said further dielectric layer overlying said vias and interposed between said vias and said stress relief layer.

2. (Original) The apparatus of Claim 1, wherein said first dielectric layer includes a layer of a first dielectric material and a layer of a second dielectric material overlying said layer of first dielectric material.

3. (Original) The apparatus of Claim 2, wherein said first dielectric material is an oxide material and said second dielectric material is a nitride material.

4. (Cancelled)

5. (Currently Amended) The apparatus of Claim [4] 1, including a cap layer overlying said vias and interposed between said vias and said further dielectric layer.

6. (Original) The apparatus of Claim [4] 1, wherein said further dielectric layer is an oxide layer.

7. (Original) The apparatus of Claim 1, including a metallic laser fuse layer overlying said dielectric layer.

8. (Original) The apparatus of Claim 7, wherein said dielectric layer includes a layer of a first dielectric material and a layer of a second dielectric material overlying said layer 5 of first dielectric material.

9. (Original) The apparatus of Claim 7, wherein said metallic fuse layer is one of aluminum and copper.

10. (Original) The apparatus of Claim 1, wherein said stress relief layer includes a further dielectric layer.

11. (Original) The apparatus of Claim 10, wherein said further dielectric layer includes a low-k material.

12. (Original) The apparatus of Claim 11, wherein said low k material is a silicon low k material.

13. (Original) The apparatus of Claim 1, wherein said first dielectric layer includes one 15 of an oxide layer and a nitride layer.

14. (Original) The apparatus of Claim 1, wherein a thickness of said stress relief layer is approximately half of a thickness of said first dielectric layer.

15. (Original) The apparatus of Claim 1, wherein a thickness of said stress relief layer is less than half of a thickness of said first dielectric layer.

16. (Original) The apparatus of Claim 1, including a further dielectric layer underlying said stress relief layer, wherein said further dielectric layer is more flexible than said first dielectric layer, and wherein said vias are embedded in said further dielectric layer.

17. (Original) The apparatus of Claim 1, wherein said vias are copper vias.

18. (Original) The apparatus of Claim 1, including a first cap layer overlying said vias and interposed between said vias and said stress relief layer.

19. (Original) The apparatus of Claim 18, including a further cap layer overlying said stress relief layer and interposed between said stress relief layer and said first dielectric layer.

20. (Original) The apparatus of Claim 19, wherein said first dielectric layer includes a layer of a first dielectric material and a layer of a second dielectric material overlying said layer of first dielectric material.

21. (Original) The apparatus of Claim 19, including a further dielectric layer that is less flexible than said stress relief layer, said further dielectric layer overlying said vias and interposed between said first cap layer and said stress relief layer.

22. (Original) The apparatus of Claim 19, including a metallic laser fuse layer overlying said first dielectric layer.

23. (Currently Amended) A method of making a semiconductor integrated circuit, comprising:

providing a plurality of electrically conductive vias for electrically connecting metal layers of the integrated circuit;

providing in overlying relationship relative to the vias a first dielectric layer; ~~and~~

providing, in overlying relationship relative to the vias and interposed between the first dielectric layer and the vias, a stress relief layer that is more flexible than the first dielectric layer; and

providing, in overlying relationship relative to the vias and interposed between the vias and the stress relief layer, a further dielectric layer that is less flexible than the stress relief layer.

24. (Original) The method of Claim 23, wherein said step of providing a stress relief layer includes providing the stress relief layer with a thickness that is approximately half of a thickness of the first dielectric layer.

25. (Original) The method of Claim 23, wherein said step of providing a stress relief layer includes providing the stress relief layer with a thickness that is less than half of a to thickness of the first dielectric layer.

26. (Original) The method of Claim 23, wherein said step of providing a first dielectric layer includes providing a layer of a first dielectric material in overlying relationship relative to a layer of a second dielectric material.

27. (Cancelled)

28. (Original) The method of Claim 23, wherein said step of providing a stress relief layer includes providing a further dielectric layer.

29. (Original) The method of Claim 28, wherein said step of providing a further dielectric layer includes providing a layer of low-k material.